

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of :

Margaret Fyfield

Serial No. : 09/731,596

Group Art Unit : 2813

Filed : December 06, 2000

Examiner : Huynh, Yennhu B.

For : Method For Probing A
Semiconductor Wafer

Atty Docket : 100.365 / 00-103



I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Connie Del Castillo

6/10/05 *Connie del Castillo*
Date Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
408-433-7475

Respectfully submitted,

Timothy Croll
Reg. No. 36,771

Date: 10 JUN 05